

REMARKS

By the present amendment and response, claims 16 and 34 have been amended to overcome the Examiner's objections. New claims 35 and 36 have been added. New claim 35 is the independent form of claim 18, which includes all of the limitations of base claim 16. New claim 36 depends from claim 35 and corresponds to dependent claim 19. New claims 35 and 36 are thus allowable according to the Examiner's comments on page 5 of the Final Office Action dated December 30, 2002. Thus, claims 16-36 remain in the present application, claims 28-33 have been allowed, and claims 35 and 36 are now in condition for allowance. Reconsideration and allowance of outstanding claims 16-27 and 34 in view of the following remarks are requested.

In the *final rejection* of December 30, 2002, the Examiner has rejected claims 16, 19-27, and 34 under 35 USC §102(e) as being anticipated by U.S. patent number 6,222,269 to Tatsuya Usami ("Usami"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 16 and 34, is patentably distinguishable over Usami. However, Applicant reserves the right to provide declarations and/or documents under 37 CFR §1.131 to "swear behind" the effective filing date of Usami.

Subject to Applicant's reserved right to establish priority of the present invention under 37 CFR §1.131, Applicant submits that the present invention, as defined by amended independent claim 16, teaches, among other things, "low-k material filling all of the gaps between the metal lines" formed from a first metal layer and "a protective layer

formed directly over and in direct contact with the metal lines and the low-k material.”

As disclosed in the present application, the metal lines formed in the first metal layer have gaps formed between them (i.e. the metal lines) and the low-k material fills all of the gaps.

As disclosed in the present application, the protective layer is formed directly over and in direct contact with the metal lines and the low-k material that fills all of the gaps between the metal lines. Thus, no other layer or material is situated between the protective layer and the metal lines and low-k material. As a result, the protective layer formed directly over and in direct contact with the metal lines and the low-k material that is situated between the metal lines provides an etch stop that protects the low-k material from chemicals utilized to etch vias in the dielectric layer situated above the metal lines. As such, the protective layer prevents the undesirable formation of poisoned vias that can occur when the low-k material situated in gaps between the metal lines is exposed to chemicals utilized to etch the vias. Thus, by utilizing low-k material situated in all of the gaps between metal lines and a protective layer directly over and in direct contact with the metal lines and the low-k material, the present invention advantageously achieves an interconnect having reduced interconnect capacitance without suffering the undesirable effects of poisoned vias.

In contrast, Usami does not teach, disclose, or suggest “low-k material filling all of the gaps between the metal lines” formed from a first metal layer and “a protective layer formed directly over and in direct contact with the metal lines and the low-k material.”

Usami specifically discloses an interconnect comprising a plurality of lower interconnect lines 3 formed on first stopper layer 2, which is formed on thick insulating layer 1 on the surface of a semiconductor substrate. See, for example, column 5, lines 55-65 and Figure 1 of Usami. In Usami, first interlevel insulator 4 is formed in a widely spaced region between adjacent lower interconnect lines 3, while low dielectric constant layer 5 is formed in a narrowly spaced region between adjacent lower interconnect lines 3. See, for example, column 5, lines 66-67, column 6, lines 1-2 and Figure 1 of Usami. Thus, in Usami, low dielectric constant layer 5 is formed only in narrowly spaced regions between adjacent lower interconnect lines 3, not in widely spaced regions. Thus, in Usami, low dielectric constant layer 5 is situated in gaps or spaces between some of adjacent lower interconnect lines 3, while first interlevel insulator 4 is situated in gaps or spaces between other adjacent lower interconnect lines 3.

Furthermore, in Usami, an interlevel insulator having a small coefficient of thermal expansion and high strength is used in the widely spaced region between interconnect lines to overcome the problem of crack generation which would take place if a low-dielectric constant insulating layer were used in all the regions (both widely and narrowly spaced regions) as an interlevel insulator. See, for example, Usami, column 8, lines 21-27. Thus, Usami teaches against using a low dielectric constant layer in all of the regions between interconnect lines.

Additionally, in Usami, second interlevel insulator 6 is situated over interconnect lines 3, first interlevel insulator 4, and low dielectric constant insulating layer 5. See, for

example, column 6, lines 10-13 and Figure 1 of Usami. Second stopper layer 7 is situated over second interlevel insulator 6, and third interlevel insulator 8 is situated over second stopper layer 7. See, for example, column 6, lines 10-13 and Figure 1 of Usami. Second interlevel insulator 6 and third interlevel insulator 8 are composed of silicon dioxide or the like having a low hygroscopicity. See, for example, Usami, column 6, lines 18-21. Thus, in Usami, a dielectric layer, i.e. second interlevel insulator 6, is situated directly over interconnect lines 3, first interlevel insulator 4, and low dielectric constant insulating layer 5, and a protective layer, i.e. second stopper layer 7, is situated over second interlevel insulator 6. Thus, since second interlevel insulator 6 separates the protective layer, i.e. second stopper layer 7, from interconnect lines 3 and low dielectric constant insulating layer 5, the protective layer is not situated directly over and in direct contact with interconnect lines 3 and low dielectric constant insulating layer 5.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 16, is not suggested, disclosed, or taught by Usami. As such, the present invention, as defined by amended independent claim 16, is patentably distinguishable over Usami. Thus, claims 17-27 depending from amended independent claim 16 are, *a fortiori*, also patentably distinguishable over Usami for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by amended independent claim 34, teaches, among other things, “material filling all of the gaps between the metal lines” formed from


a first metal layer and “a protective layer formed directly over and in direct contact with the metal lines and the material.” For the same reasons as discussed above, the invention, as defined by amended independent claim 34, is not suggested, disclosed, or taught by Usami. Thus, the present invention, as defined by amended independent claim 34, is also patentably distinguishable over Usami.

In the *final rejection* of December 30, 2002, the Examiner has further rejected claims 21, 22, 25, and 27 under 35 USC §103(a) as being unpatentable over Usami. As discussed above, amended independent claim 16 is patentably distinguishable over Usami and, as such, claims 21, 22, 25, and 27 depending from amended independent claim 16 are, *a fortiori*, also patentably distinguishable over Usami for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 16 and 34 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, dependent claims 17-27 are also patentably distinguishable over the art cited by the Examiner. For all the foregoing reasons, an early allowance of outstanding claims 16-27 and 34 and an early Notice of Allowance for all pending claims 16-36 is respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 5/30/03


Michael Farjami, Esq.
Reg. No. 38, 135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop RCE; Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: 5/30/03

Lori Llave
Name of Person Mailing Paper and/or Fee

Lori Llave 5/30/03
Signature Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 16 and 34 have been amended as follows:

16. (Thrice Amended) An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling all of the gaps between the metal lines and having a height and one or more vertical portions;

(c) a protective layer formed directly over ⁽⁶⁾ and in direct contact with the metal lines and the low-k material, wherein the protective layer covers at least one vertical portion of the low-k material;

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer ⁽¹⁾ has a different composition than the low-k material and the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal vias to contact the first metal lines.

34. (Twice Amended) An interconnect comprising:

- (a) a plurality of metal lines formed from a first metal layer, said metal lines having gaps therebetween;
 - (b) material filling all of the gaps between the metal lines and having a height and one or more vertical portions;
 - (c) a protective layer formed directly over and in direct contact with the metal lines and the material, wherein the protective layer covers at least one vertical portion of the material;
 - (d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the protective layer;
 - (e) one or more vias etched in the dielectric layer;
 - (f) a metal within the vias;
 - (g) a second metal layer formed over and in direct contact with the dielectric layer;
- and
- (h) one or more openings in the protective layer for allowing the metal in the vias to contact the metal lines.